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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,370	04/01/2004	Chih Chieh Yeh	MXIC 1571-1	8260

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EXAMINER	
PHAN, TRONG Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,370	YEH ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In view of the newly discovered art of Kobatake, 5,815,441, the allowance of claims 1-65 as set forth in the last office action of May 9, 2005 has been withdrawn.

A new non-final office action has been set forth as below:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walukas, 6,229,737, in view of Kobatake, 5,815,441, and Lin, 6,671,209.

Walukas, 6,229,737, discloses in Fig. 1 a memory device comprising :

first memory array EEPROM 12 for storing a page of data (see lines 44-45, column 5) in response to a first interleaving algorithm (se lines 1-3, column 5);

second flash memory array 14 for storing a data bite (see lines 39-42, column 6) in response to a second interleaving algorithm (see lines 3-6, column 5);

processor CPU 24;

SRAM 22.

What is not shown in Walukas, 6,229,737, is the first and the second memory array on the same substrate as recited in claims 1, 21-23 and 45-46.

Kobatake, 5,815,441, discloses in Fig.1 the teaching of forming a first nonvolatile EEPROM 16 and a second nonvolatile Flash memory array 17 on the same substrate in

a single chip (see lines 30-48, column 2).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to form first memory array EEPROM 12 and second flash memory array 14 in Fig. 1 of Walukas, 6,229,737, on the same substrate in a single chip as taught by Fig. 1 of Kobatake, 5,815,441, for the purpose of having low cost in which programs and data can be stored separately (see lines 30-34, column 2 of Kobatake, 5,815,441).

What is not shown in Walukas, 6,229,737, which is modified by Kobatake, 5,815,441, is the charge storage non-volatile memory cells as recited in claims 2-20, 24-44 and 47--65.

Lin, 6,671,209, discloses in Fig. 1 a memory cell which can be used for EEPROM and Flash memory devices (see lines 18-43, column 1) comprising:

substrate 10;

charge trapping layer 16 of silicon nitride;

first tunneling oxide layer 14;

second dielectric layer 18;

gate electrode 20;

source channel region 22;

drain channel region 24;

erasing by band-to-band hot electron/holes/electric field injection (see lines 44-51, column 1 and lines 31-32, column 2);

two-bit per single cell (see lines 17-20, column 2).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the memory cell in Fig. 1 of Lin, 6,671,209, for the EEPROM array 12 and the Flash memory array 14 in Fig. 1 of Walukas et al., 6,229,737, which is modified by Kobatake, 5,815,441, for the purpose of preventing drain leakage current and reducing power consumption (see lines 11-17, column 2 of Lin, 6,671,209).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zabrabian can be reached on (571)272-1851. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

phan Trong

TRONG PHAN
PRIMARY EXAMINER